CLAIMS

What is claimed is:

1. A method for performing logical transformations for global routing in an integrated circuit design, comprising steps of:

(a) determining whether homeomorphism exists between logic trees A and B; and

(b) when homeomorphism exists between said logic trees A and B, assigning same coordinates to nodes of degree != 2 of said logic trees A and B for optimizing design parameters.

2. The method of claim 1, wherein said step (a) comprises:

(a1) assigning a value n to a parameter fixed_corr of Na and Nb for a n-th pair (Na, Nb), where Na is a marked node of said logic tree A, Nb is a marked node of said logic tree B, and Na is a corresponding node of Nb; assigning NO_FIXED_CORR value to fixed_corr for all nodes of said logical trees A and B that are not in pairs of corresponding nodes; and returning an error code when there are marked nodes in said logical tree B for which no corresponding nodes in said logical tree A exist.

3. The method of claim 2, wherein said step (a) further comprises:

(a2) assigning a code (a pair (I, a_1 a_2 ... a_I) to a node N of said logic trees A and B, where I is a length and a_1 ... a_I is an array of integers.

4. The method of claim 3, wherein in said step (a2):

i) when N is a variable, said code is (1, variable number);

ii) when N is a constant, said code is (1, -1); and

iii) when N has children and codes of children are determined as follows:

a) when all children have the code (1, -l), the same code (1, -l) is assigned to N; and

b) (1) when there are several children that are variables with the same variable number, one may leave only one of these children;

(2) when only one significant (i.e., with a code different from (1, -1)) child is left after said (1), and this child has a code (I, a_1 ... a_I), the same code is assigned to N if N.fixed_corr == NO_FIXED_CORR; otherwise, code (I+2, 1 N.fixed_corr a_1 ... a-I) is assigned to N; and

(3) when several significant children are left after said (1), and codes of these children are (I_1, c_1) ... (I_k, c_k) (k >= 2) (c_j = a_j,1 ... a_j,c_j), these codes are ordered lexicographically (c_j(1) <= c_j(2) <= ... <= c_j(k)) and code (I_1 + ... + I_k + 2, k N.fixed_corr I_j(1) ... I_j(k) c_j(1) ... c_j(k)) is assigned to N.

5. The method of claim 4, wherein said step (a) further comprises:

(a3) establishing homeomorphism between said logic trees A and B when root nodes of said logical tress A and B have the same code.

6. The method of claim 1, wherein said step (b) comprises:

(b1) clearing all space occupied by said logical tree A;

(b2) assigning corr_node fields for nodes of said logical trees A and B with (number of children != 1) or (fixed_corr != NO_FIXED_CORR) in the following way: corr_nodes should have the same code; assigning corr_node only

for one of these variables when a node has several children that are variables with the same variable number; assign corr_node = NULL for nodes with fixed_corr = NO_FIXED_CORR and children number = 1; and returning an error code when one fails to assign corr_node to some nodes;

(b3) assigning coordinates to nodes N of said logic tree B with the number of children >= 2 or with fixed_corr != NO_FIXED_CORR; assigning a routing tree to N.corr_node; and changing free space to show that a node is added to a field;

(b4) slightly changing correspondence (corr_nodes) for variables to achieve the following: routing positions of corresponding variables should coincide; and for variables with NULL corr_node in said logic tree B, putting routing posiotion = -1;

(b5) assigning variable trees as follows: for each variable, merging a tree of these variables with routing trees of all nodes from said logic tree A that have the only child;

(b6) when a node of said logic tree A has several children that are variables with the same variable number, deleting parts of this variable's routing tree that corresponds to these children except one that does not have NULL corr_node;

(b7) inserting nodes N of said logic tree B with the number of children = 1;

(b8) assigning routing positions to variables that have routing position = -1;

(b9) re-computing delays and caps; and

(b10) clearing a space occupied by said logical tree B, putting back nodes of said logical tree A, and returning a result: an error code or a success code, wherein when the result is a success code, all nodes of B have correct coordinates and routing trees assigned.

7. An apparatus for performing logical transformations for global routing in an integrated circuit design, comprising:

(a) means for determining whether homeomorphism exists between logic trees A and B; and

(b) when homeomorphism exists between said logic trees A and B, means for assigning same coordinates to nodes of degree != 2 of said logic trees A and B for optimizing design parameters.

8. The apparatus of claim 7, wherein said means (a) comprises:

(a1) means for assigning a value n to a parameter fixed_corr of Na and Nb for a n-th pair (Na, Nb), where Na is a marked node of said logic tree A, Nb is a marked node of said logic tree B, and Na is a corresponding node of Nb; means for assigning NO_FIXED_CORR value to fixed_corr for all nodes of said logical trees A and B that are not in pairs of corresponding nodes; and means for returning an error code when there are marked nodes in said logical tree B for which no corresponding nodes in said logical tree A exist.

9. The apparatus of claim 8, wherein said means (a) further comprises:

(a2) means for assigning a code (a pair (I, a_1 a_2 ... a_I) to a node N of said logic trees A and B, where I is a length and a_1 ... a_I is an array of integers.

10. The apparatus of claim 9, wherein in said means (a2):

i) when N is a variable, said code is (1, variable number);

ii) when N is a constant, said code is (1, -1); and

iii) when N has children and codes of children are determined as follows:

a) when all children have the code (1, -l), the same code (1, -l)

is assigned to N; and

b) (1) when there are several children that are variables with the same variable number, one may leave only one of these children;

(2) when only one significant (i.e., with a code different from (1, -1)) child is left after said (1), and this child has a code (I, a_1 ... a_I), the same code is assigned to N if N.fixed_corr == NO_FIXED_CORR; otherwise, code (I+2, 1 N.fixed_corr a_1 ... a-I) is assigned to N; and

(3) when several significant children are left after said (1), and codes of these children are (I_1, c_1) ... (I_k, c_k) (k >= 2) (c_j = a_j,1 ... a_j,c_j), these codes are ordered lexicographically (c_j(1) <= c_j(2) <= ... <= c_j(k)) and code (I_1 + ... + I_k + 2, k N.fixed_corr I_j(1) ... I_j(k) c_j(1) ... c_j(k)) is assigned to N.

11. The apparatus of claim 10, wherein said means (a) further comprises:

(a3) means for establishing homeomorphism between said logic trees A and B when root nodes of said logical tress A and B have the same code.

12. The apparatus of claim 7, wherein said means (b) comprises:

(b1) means for clearing all space occupied by said logical tree A;

(b2) means for assigning corr_node fields for nodes of said logical trees A and B with (number of children != 1) or (fixed_corr != NO_FIXED_CORR) in the following way: corr_nodes should have the same code; means for assigning corr_node only for one of these variables when a node has several children that are variables with the same variable number; means for assign corr_node = NULL for nodes with fixed_corr = NO_FIXED_CORR and

children number = 1; and means for returning an error code when one fails to assign corr_node to some nodes;

(b3) means for assigning coordinates to nodes N of said logic tree B with the number of children >= 2 or with fixed_corr != NO_FIXED_CORR; means for assigning a routing tree to N.corr_node; and means for changing free space to show that a node is added to a field;

(b4) means for slightly changing correspondence (corr_nodes) for variables to achieve the following: routing positions of corresponding variables should coincide; and for variables with NULL corr_node in said logic tree B, means for putting routing posiotion = -1;

(b5) means for assigning variable trees as follows: for each variable, merging a tree of these variables with routing trees of all nodes from said logic tree A that have the only child;

(b6) when a node of said logic tree A has several children that are variables with the same variable number, means for deleting parts of this variable's routing tree that corresponds to these children except one that does not have NULL corr_node;

(b7) means for inserting nodes N of said logic tree B with the number of children = 1;

(b8) means for assigning routing positions to variables that have routing position = -1;

(b9) means for re-computing delays and caps; and

(b10) means for clearing a space occupied by said logical tree B, means for putting back nodes of said logical tree A, and means for returning a result: an

error code or a success code, wherein when the result is a success code, all nodes of B have correct coordinates and routing trees assigned.

13. A computer-readable medium having computer-executable instructions for performing a method for performing logical transformations for global routing in an integrated circuit design, said method comprising steps of:

(a) determining whether homeomorphism exists between logic trees A and B; and

(b) when homeomorphism exists between said logic trees A and B, assigning same coordinates to nodes of degree != 2 of said logic trees A and B for optimizing design parameters.

14. The computer-readable medium of claim 13, wherein said step (a) comprises:

(a1) assigning a value n to a parameter fixed_corr of Na and Nb for a n-th pair (Na, Nb), where Na is a marked node of said logic tree A, Nb is a marked node of said logic tree B, and Na is a corresponding node of Nb; assigning NO_FIXED_CORR value to fixed_corr for all nodes of said logical trees A and B that are not in pairs of corresponding nodes; and returning an error code when there are marked nodes in said logical tree B for which no corresponding nodes in said logical tree A exist.

15. The computer-readable medium of claim 14, wherein said step (a) further comprises:

(a2) assigning a code (a pair (I, a_1 a_2 ... a_I) to a node N of said logic trees A and B, where I is a length and a_1 ... a_I is an array of integers.

16. The computer-readable medium of claim 15, wherein in said step (a2):

i) when N is a variable, said code is (1, variable number);

ii) when N is a constant, said code is (1, -1); and

iii) when N has children and codes of children are determined as follows:

a) when all children have the code (1, -l), the same code (1, -l) is assigned to N; and

b) (1) when there are several children that are variables with the same variable number, one may leave only one of these children;

(2) when only one significant (i.e., with a code different from (1, -1)) child is left after said (1), and this child has a code (I, a_1 ... a_I), the same code is assigned to N if N.fixed_corr == NO_FIXED_CORR; otherwise, code (I+2, 1 N.fixed_corr a_1 ... a-I) is assigned to N; and

(3) when several significant children are left after said (1), and codes of these children are (I_1, c_1) ... (I_k, c_k) (k >= 2) (c_j = a_j,1 ... a_j,c_j), these codes are ordered lexicographically (c_j(1) <= c_j(2) <= ... <= c_j(k)) and code (I_1 + ... + I_k + 2, k N.fixed_corr I_j(1) ... I_j(k) c_j(1) ... c_j(k)) is assigned to N.

17. The computer-readable medium of claim 16, wherein said step (a) further comprises:

(a3) establishing homeomorphism between said logic trees A and B when root nodes of said logical tress A and B have the same code.

18. The computer-readable medium of claim 13, wherein said step (b) comprises:

(b1) clearing all space occupied by said logical tree A;

(b2) assigning corr_node fields for nodes of said logical trees A and B with (number of children != 1) or (fixed_corr != NO_FIXED_CORR) in the following way: corr_nodes should have the same code; assigning corr_node only for one of these variables when a node has several children that are variables

with the same variable number; assign corr_node = NULL for nodes with fixed_corr = NO_FIXED_CORR and children number = 1; and returning an error code when one fails to assign corr_node to some nodes;

(b3) assigning coordinates to nodes N of said logic tree B with the number of children >= 2 or with fixed_corr != NO_FIXED_CORR; assigning a routing tree to N.corr_node; and changing free space to show that a node is added to a field;

(b4) slightly changing correspondence (corr_nodes) for variables to achieve the following: routing positions of corresponding variables should coincide; and for variables with NULL corr_node in said logic tree B, putting routing posiotion = -1;

(b5) assigning variable trees as follows: for each variable, mering a tree of these variables with routing trees of all nodes from said logic tree A that have the only child;

(b6) when a node of said logic tree A has several children that are variables with the same variable number, deleting parts of this variable's routing tree that corresponds to these children except one that does not have NULL corr_node;

(b7) inserting nodes N of said logic tree B with the number of children = 1;

(b8) assigning routing positions to variables that have routing position = -1;

(b9) re-computing delays and caps; and

(b10) clearing a space occupied by said logical tree B, putting back nodes of said logical tree A, and returning a result: an error code or a success code, wherein when the result is a success code, all nodes of B have correct coordinates and routing trees assigned.